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# Single event effects in 0.18 $\mu\text{m}$ CMOS image sensors

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## ABSTRACT

CMOS image sensors are widely used on Earth and are becoming increasingly favourable for use in space. Advantages, such as low power consumption, and ever-improving imaging performance make CMOS an attractive option. The ability to integrate camera functions on-chip, such as biasing and sequencing, simplifies designing with CMOS sensors and can improve system reliability. One potential disadvantage to the use of CMOS is the possibility of single event effects, such as single event latchup (SEL), which can cause malfunctions or even permanent destruction of the sensor. These single event effects occur in the space environment due to the high levels of radiation incident on the sensor. This work investigates the occurrence of SEL in CMOS image sensors subjected to heavy-ion irradiation. Three devices are investigated, two of which have triple-well doping implants. The resulting latchup cross-sections are presented. It is shown that using a deep p well on 18  $\mu\text{m}$  epitaxial silicon increases the radiation hardness of the sensor against latchup. The linear energy transfer (LET) threshold for latchup is increased when using this configuration. Our findings suggest deep p wells can be used to increase the radiation tolerance of CMOS image sensors for use in future space missions.

**Keywords:** CMOS, SEE, SEL, latchup, image sensor, radiation, space

## 1. INTRODUCTION

SEL may be caused in the space environment by a range of ionising particles and is one of the potential disadvantages of using CMOS technology in space for image sensor applications.<sup>1,2</sup> The expected rate of SEL of CMOS devices must be assessed before use in space to ensure that the expected rate of events and their effects will be manageable.

### 1.1 Single Event Latchup in CMOS devices

CMOS processing allows, by definition, the fabrication of n and p channel Field Effect Transistors (FETs) on the same silicon substrate. In more advanced processes a p type substrate is usually used, but a high quality layer of epitaxial silicon (with a lower concentration of acceptor dopants) is grown onto the substrate. Wells of n type and p type silicon are then formed in the epitaxial silicon as required. Although wells may be separated to some extent by thick oxide between them (shallow trench isolation or deep trench isolation), the n and p wells usually touch each other. The cross section of the doping arrangement of a typical dual-well (i.e. using n and p wells) CMOS circuit is shown in Figure 1(a). A side effect of this implementation is that it connects the positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) supply rails via a pnpn structure which is equivalent to two Bipolar Junction Transistors (BJT) (or a thyristor). If the resistance of the wells is taken into account a parasitic circuit (Figure 1(b)) can be drawn. A similar parasitic circuit exists whenever sources are connected to the power supply, regardless of the logical connections made with the drains and gates of the FETs.

Under normal circuit operation the parasitic circuit only contributes a small leakage current from  $V_{DD}$  to  $V_{SS}$ . However, the cross-linked arrangement of the BJTs means that the collector current will be amplified by the other BJT and fed back as a base current. If the current gain,  $\beta$ , of the BJTs is such that  $\beta_{npn} \cdot \beta_{pnp} > 1$  then the circuit is bi-stable. If sufficient collector current is achieved in either BJT the current  $I_{V_{DD}}$  will increase until it is limited by either the internal resistances of the chip or by the power supply. This runaway current

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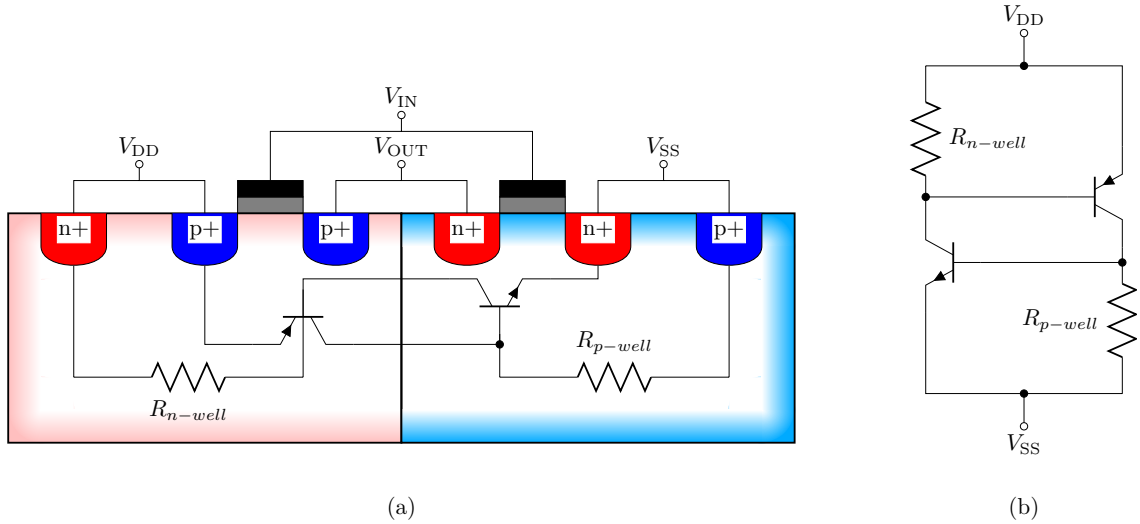


Figure 1. (a) Cross section of the inverter circuit as fabricated in dual-well CMOS (after<sup>3</sup>). (b) The parasitic circuit between  $V_{DD}$  and  $V_{SS}$  which is responsible for latchup.

condition is known as a latchup. Stopping (or quenching) the latchup requires intervention to reduce the supply current. The current to trigger a latchup condition can be provided either by a disturbance in supply voltage (e.g. from electrostatic discharge into the device) or by the introduction of a cloud of free charge carriers in the wells through ionising radiation. Latchup, when triggered by an incoming particle, is called Single Event Latchup (SEL).

## 1.2 Latchup hardening

To prevent or reduce the susceptibility of CMOS circuits to latchup several techniques can be used at design level.

- The supply voltage can be reduced. In fact the supply voltage (as opposed to the LET) at which latchup occurs is often used as a metric when comparing designs.<sup>4</sup>
- SEL can be controlled with a Current Limiting Device (CLD) (see<sup>5</sup> for example) which is generally on-chip circuitry which will automatically quench latchups by reducing the current when they occur. This adds area and complexity to the design.
- The potential structure within the device can be controlled thus diverting the charge cloud away from sensitive areas.
- Recombination rates can be increased by reducing the field in which the charge cloud is created.
- Decreasing the well or substrate resistances increases the current required to forward bias the base-emitter junctions.<sup>4</sup>
- Certain technologies are intrinsically immune to latchup. For example Silicon On Insulator (SOI) is often assumed to be latchup immune<sup>6,7</sup> but the exact technology must be examined. For example, some BiCMOS technologies do have a pnpn path from  $V_{DD}$  to  $V_{SS}$ .
- Triple wells are formed when a layer of n or p doping is implanted under the usual wells. An example of the deep n well and deep p well implementations is shown in Figure 2. Triple wells have been shown to reduce SEL<sup>8,9</sup> in some situations. The inclusion of a triple well option, which is common in processes of  $\leq 0.18\mu\text{m}$ , originally had the purpose of allowing back-biasing and noise isolation in analogue and Radio Frequency (RF) circuits.<sup>10</sup>

There are at least two important competing effects of using triple wells. For example, the deep n well connects multiple n wells which significantly reduces the resistance to the BJT base<sup>8</sup> and reduces the pnp BJT gain. However the deep n well has the opposite effect on the npn BJT, whose base to  $V_{SS}$  resistance and gain increase.<sup>10</sup> Uemura *et al*<sup>11</sup> explored some of the ways in which SEL can be reduced through the use of deep n wells and deep p wells and increasing the doping of the triple wells. In the SRAM devices (50 nm and 90 nm processes) tested with neutron irradiation, those with deep p wells showed the best resistance to SEL and they did not show the increased SEU rate associated with deep n wells. Deep p wells were shown in<sup>12</sup> to harden against SEL from neutrons and this effect is explored with a 3D TCAD simulation.

The effect of epitaxial thickness on LET threshold was investigated experimentally in<sup>13</sup> and.<sup>1</sup> It was demonstrated that increasing the epitaxial layer thickness from 9  $\mu\text{m}$  to 12  $\mu\text{m}$  decreased the LET threshold. A good summary of strategies for SEL hardening can be found in.<sup>4</sup>

## 2. DEVICES

### 2.1 e2v Sapphire and Ruby sensors

The e2v Sapphire 1.3M and Ruby 1.3M sensors are 1.3 megapixel front illuminated CMOS image sensors with 5.6  $\mu\text{m}$  square pixels.<sup>14,15</sup> Variants in 3T (rolling shutter) or 4T (global shutter) are available. The Ruby shares the same digital circuitry as the Sapphire. However, the Ruby has enhanced near infra-red QE.

### 2.2 Test device variants

Three device variants were provided by e2v. The first of these is a standard Sapphire device, the second a special Sapphire device with a Deep N-Well (DNW). The third device was a Ruby sensor with Deep P-Well (DPW) on 18  $\mu\text{m}$  thick epitaxial silicon. Since the image area only has n channel transistors it is not subject to latchup. SEUs, however, are possible in the image array and would appear as spurious pixel values. The design of the image array is the only difference in the layout between the Sapphire and Ruby devices. Therefore, only the process modifications (summarised in Table 1) affect the SEE sensitivity of the different sensors. The structures of the four test devices are shown in Figure 2.

Device	Epi thickness ( $\mu\text{m}$ )	Epi resistivity ( $\Omega\text{ cm}$ )	Buried layer	Remarks
Sapphire	5.5	30	No	
Deep n well Sapphire	5.5	30	DNW	DNW added under 1.8V standard cells
Ruby 18 $\mu\text{m}$	18	1000	DPW	DPW added under all circuits except pixels

Table 1. Details of the device variants used for SEL testing

## 3. EXPERIMENTAL SETUP

### 3.1 The heavy ion facility at Université Catholique de Louvain

The heavy ion irradiation in this work was carried out at the Cyclone cyclotron at the Heavy Ion Facility (HIF) of the Université Catholique de Louvain.

Table 2 shows the ion species, energies, LET and range of the heavy ions available in the high range cocktail at the HIF. This information is provided by the HIF<sup>16</sup> except the effective LETs at beam inclinations of 30°, 45° and 60° which are calculated from equation 1.

$$LET_{eff} = LET \sec \theta \quad (1)$$

The high range cocktail uses a mass to charge ratio of  $m/q \simeq 3.33$ . A different cocktail is available using  $m/q \simeq 5$  which allows a slightly higher maximum pure LET of 69.2 MeV  $\text{cm}^2\text{mg}^{-1}$ . However, the higher range cocktail allows high effective LETs and the greater range means high tilt angles can be used if necessary.

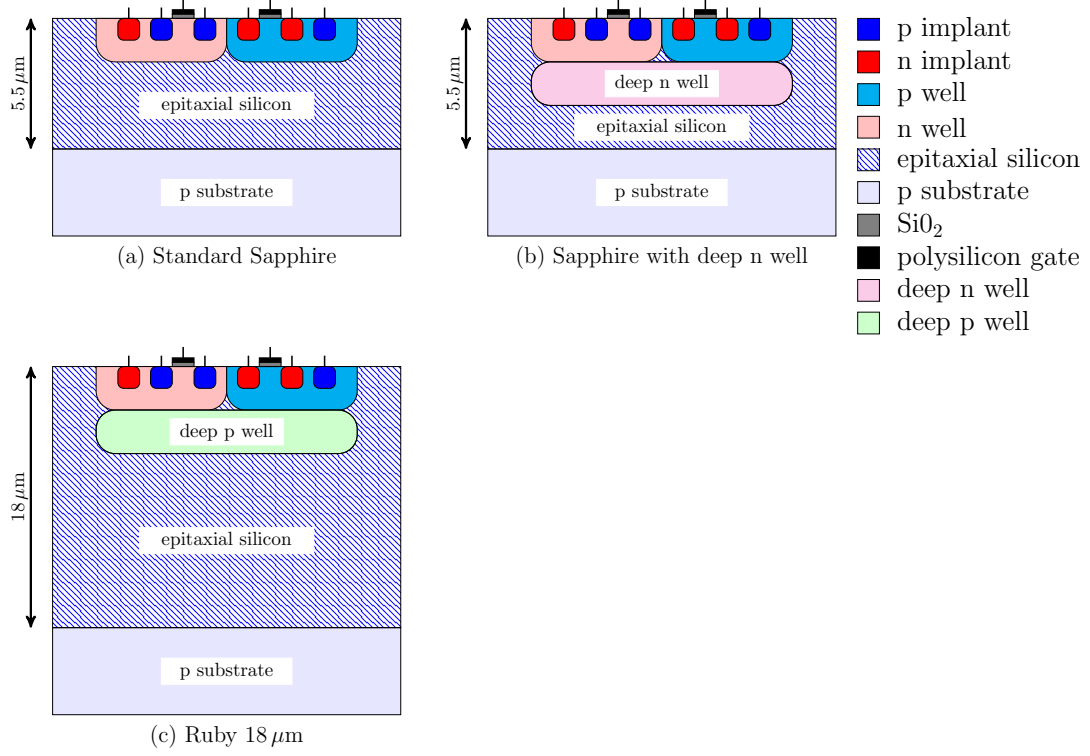


Figure 2. Simplified cross sections of the three device variants listed in table 1. The differences between the devices are the presence of deep n or p wells and the thickness of the high resistivity epitaxial silicon layer. The deep wells are not present under the imaging area on any of the devices.

m/q	Ion	Energy on DUT (MeV)	Range in Si ( $\mu\text{m}$ )	LET in Si ( $\text{MeV cm}^2\text{mg}^{-1}$ )	Effective LET ( $\text{MeV cm}^2\text{mg}^{-1}$ )		
					30°	45°	60°
3.25	$^{13}\text{C}^{4+}$	131	269.3	1.3	1.5	1.8	2.6
3.5	$^{14}\text{N}^{4+}$	122	170.8	1.9	2.2	2.7	3.8
3.14	$^{22}\text{Ne}^{7+}$	238	202	3.3	3.8	4.7	6.6
3.33	$^{40}\text{Ar}^{12+}$	379	120.5	10.0	11.5	14.1	20.0
3.218	$^{58}\text{Ni}^{18+}$	582	100.5	20.4	23.6	28.8	40.8
3.35	$^{84}\text{Kr}^{25+}$	769	94.2	32.4	37.4	45.8	64.8
3.54	$^{124}\text{Xe}^{35+}$	995	73.1	62.5	72.2	88.4	125.0

Table 2. Heavy ion species available in the high range (high energy) cocktail at the HIF ( $m/q \simeq 3.33$ )

### 3.2 C3D camera board

The camera system used for running the sensors in this experiment was the Compact CMOS Camera Demonstrator (C3D).<sup>17</sup> The C3D camera was initially designed to run on board the UKube-1 CubeSat mission, launched in July 2014. Aboard UKube-1 the C3D ran three Sapphire devices: two for imaging and one for studying radiation damage in the sensor. The C3D camera was used previously for SEL testing of standard Sapphire sensors at LETs from  $10 \text{ MeV.cm}^2/\text{mg}$  to  $25 \text{ MeV.cm}^2/\text{mg}$ . In flight mode the C3D board interfaces with the spacecraft I<sup>2</sup>C bus. Simple I<sup>2</sup>C commands sent from the spacecraft are executed by the Altera FPGA running on the C3D and the FPGA controls each of the image sensors and image data return to the spacecraft. By using a USB to I<sup>2</sup>C converter board and modifying the firmware on the FPGA the C3D becomes a convenient system for running Sapphire or Ruby sensors from a PC. The C3D board mounted in the vacuum chamber at the HIF is shown in Figure 3.

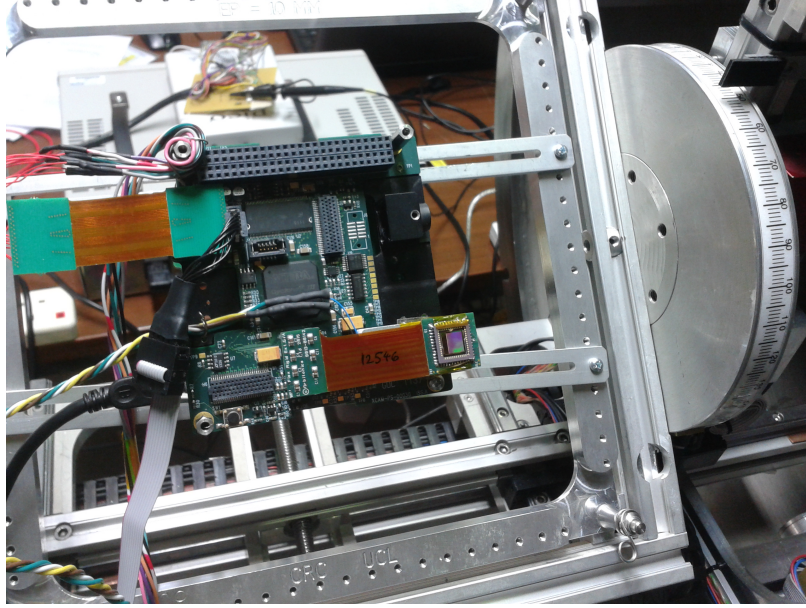


Figure 3. The test board with sensor mounted, awaiting shielding, before being placed in the beam. The motor to rotate the board is shown on the right. The angle of rotation is visible to the operator via a camera system to the control room.

### 3.3 Experimental setup

A high level schematic of the entire test system including those parts of the HIF used is shown in Figure 4.

Once in the beam the sensors performed regular operations requested by the code in order to measure SEUs and to simulate typical device usage. Current draw in each of the three sensor supplies (1.8 V analogue, 1.8 V digital and 3.3 V analogue) was measured on a  $1\Omega$  sense resistor. The 1.8 V digital circuits in the sensor are those using CMOS logic and are therefore most likely to suffer from SEL.

Supply current was recorded on a Picologger ADC-20 connected to a PC. Whenever a current draw of more than 50 mA was detected (due to a latchup) by software on the PC a reset command was sent to the FPGA on the C3D board. On receipt of the reset command the FPGA I/O operated FET switches to disconnect all three power supplies from the sensor in order to quench the latchup. The FPGA then reset the sensor and re-configured the sensor's internal registers before resuming steady state operations. SEU information was downloaded from the FPGA every six seconds and the download was completed even in the event of a latchup. The current was sampled every second. Each time a latchup occurred it took up to six seconds before the reset operation was carried out. The delay before reset was in order to download every SEU log. The SEL rate was measured whilst the sensors were under irradiation and where necessary the ion flux was adjusted to bring the SEL rate within a sensible range (an average of one SEL event every 10 to 20 seconds). This was a good compromise between the uncertainty on rate determination given by the sampling interval of 1 second and the uncertainty given by a low number of events. Once a suitable flux was adopted at each LET the policy was to use a run time of 20 minutes, or up to 100 latchup events, whichever was the soonest. The flux at the HIF can be adjusted from  $10^1$  ions/cm<sup>2</sup>.s to  $10^4$  ions/cm<sup>2</sup>.s.<sup>16</sup>

Figure 5 shows an example current log taken. The 50 mA detection threshold is marked with a dashed line. To calculate the latchup cross-sections, the dead time was removed from the current log time series data. The time during which latchup could occur was measured as the time between resets and latchups.

### 3.4 Temperature measurement

In order to measure the temperature of the sensor, a block of aluminium was built onto the C3D board as shown in Figure 6. A Platinum Resistance Thermometer (PRT) was fixed to the block and the sensors were attached to the block. Temperature at the PRT was logged using the Picologger.

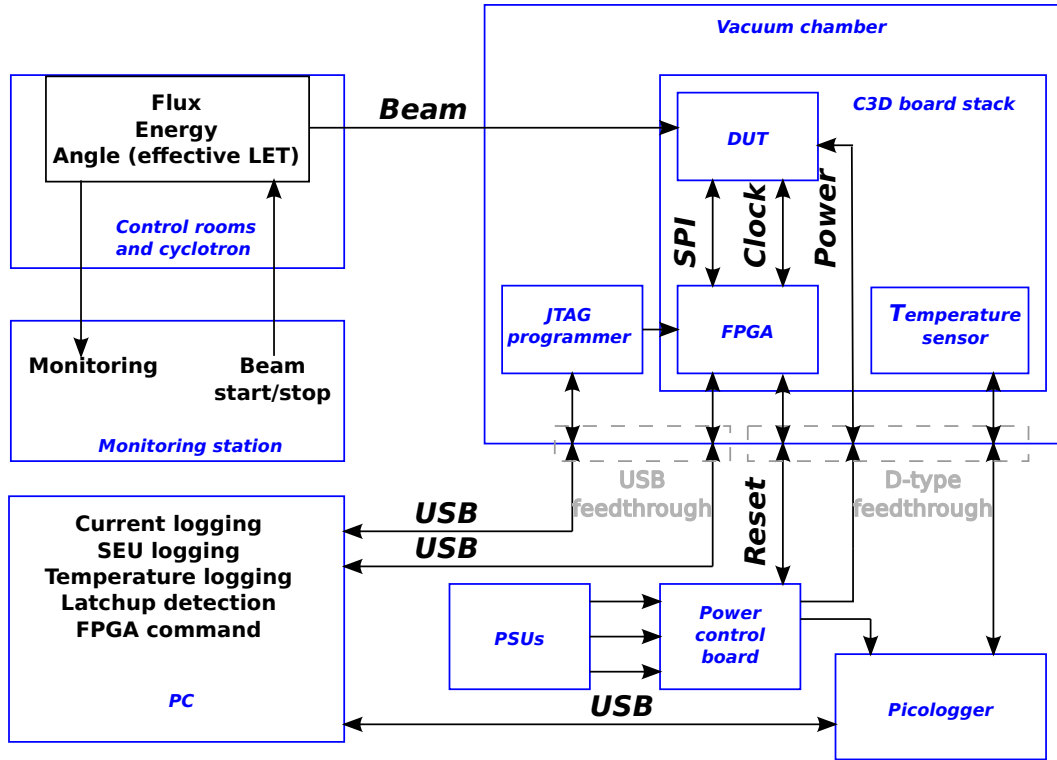


Figure 4. The experimental setup. The current measurement of the 3 power supplies to the device was performed on the power control board.

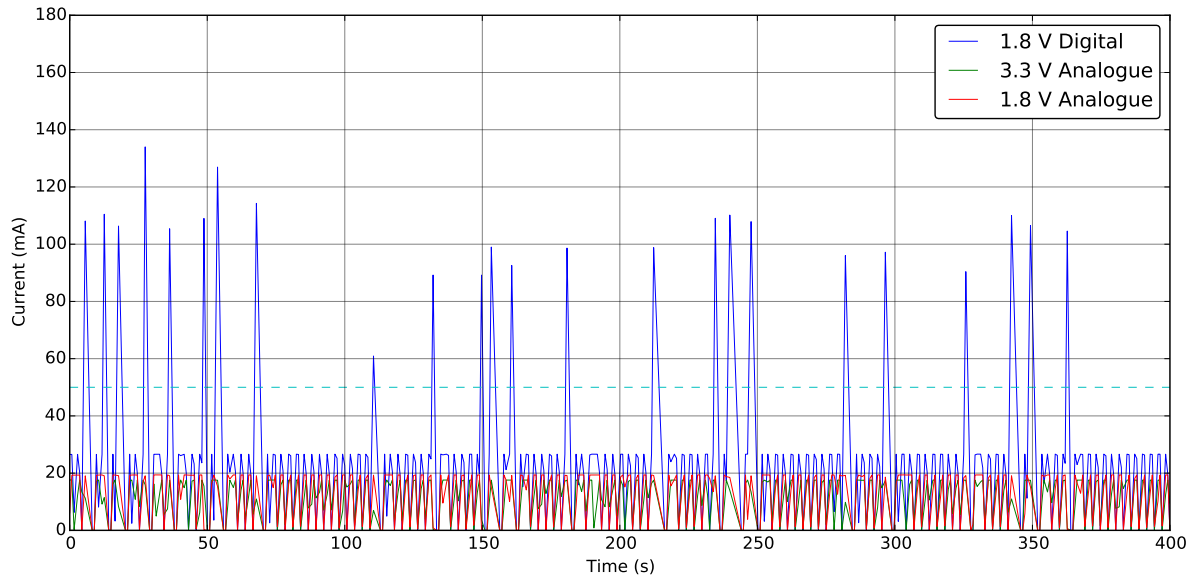


Figure 5. Example current log for all three supplies. The dashed line shows the SEL detection threshold of 50 mA.



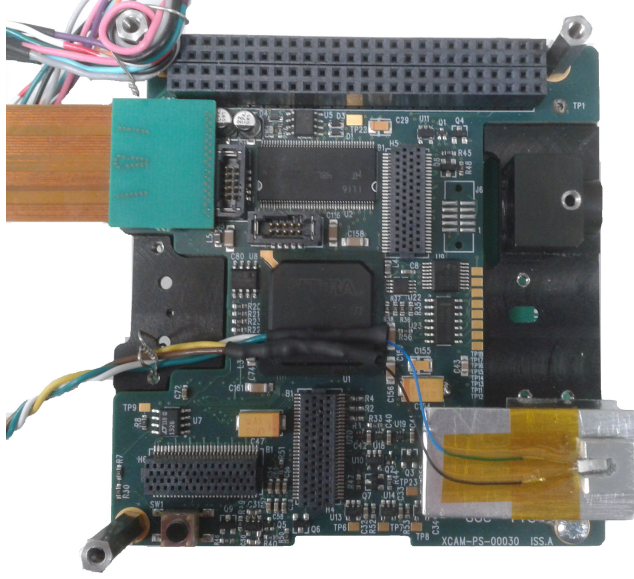


Figure 6. The C3D board. The sensor is not mounted yet and the PRT fixed to the aluminium block is shown.

## 4. SEL RESULTS AND ANALYSIS

### 4.1 Cross sections and extraction of threshold LET

The measured SEL cross sections for the four devices are plotted in Figure 8. Some data points, for LETs where no SELs occurred, are not shown because of the logarithmic axis.

The cross section is given by

$$\sigma = \frac{\text{latchup rate}}{\text{ion flux}} \quad (2)$$

where the latchup rate is in latchups/s and the flux is in ions/cm<sup>2</sup>s.

SEL cross section as a function of LET is usually modelled using the Weibull cumulative distribution function<sup>19</sup>

$$\sigma(L_i) = \sigma_0 \left( 1 - \exp \left[ - \left( \frac{L_i - L_0}{W} \right)^S \right] \right) \quad (3)$$

where  $L_i$  is the LET,  $L_0$  is the threshold LET,  $\sigma_0$  is the saturation cross-section, and  $W$  and  $S$  are fitting parameters. This model provides two parameters for characterising SEL susceptibility: The saturation cross section,  $\sigma_0$ , which is the maximum possible cross section for any value of LET; and the threshold LET,  $L_0$ , which is the LET below which SEL events do not occur. Such Weibull fits to the data, using a weighted least-mean-squares fit, are shown in Figure 8. The fitting parameters used are given in table 3. The fits are to all data points, including at LETs where no SEL events occurred. The shaping parameter  $S$  has been constrained to  $S \geq 1$  which implies that latchups become more likely with LET (as evidenced by the data).

Device	$\sigma_0$ (latchups/ion/cm <sup>2</sup> )	$L_0$ (MeV.cm <sup>2</sup> /mg)	$W$ (MeV.cm <sup>2</sup> /mg)	$S$
Sapphire	$2.19 \times 10^{-3}$	3.71	39.9	6.83
DNW Sapphire	$2.76 \times 10^{-3}$	6.79	30.8	3.45
Ruby 18 $\mu\text{m}$	$1.80 \times 10^{-3}$	18.1	29.5	3.36

Table 3. Fitting parameters which provide the curves in Figure 7. Here,  $W$  and  $S$  are chosen independently for each device.

The characteristics described by Table 3 imply that LET thresholds increase in the order: Sapphire; DNW Sapphire; Ruby 18  $\mu\text{m}$ . The saturation cross sections are in the reverse order. The order of LET thresholds is



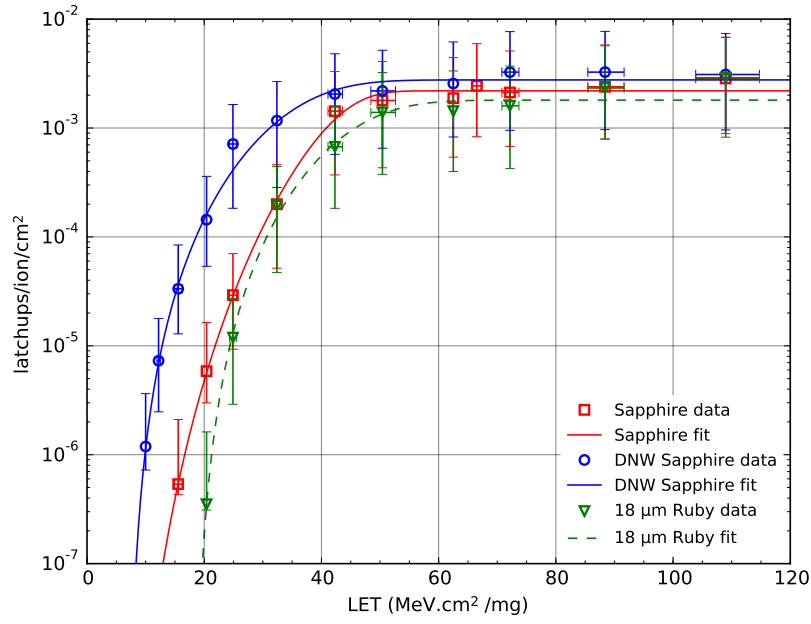


Figure 7. The SEL cross section data. Also shown are Weibull fits to the data, calculated with  $\sigma_0$ ,  $L_0$ ,  $W$  and  $S$  as free parameters. In the experiment the Sapphire began to latchup at a higher LET than the DNW Sapphire. However, because of the shape of the curve, the threshold LET is calculated to be lower. Error bars are based on 10% uncertainty of flux, angle of incidence uncertainty of  $2^\circ$ , and the uncertainty introduced by the finite number of latchups, according to.<sup>18</sup>

interesting, because it places the LET threshold of the DNW Sapphire higher than the LET threshold of the Sapphire, even though the impression given by the data is that the Sapphire has a higher LET threshold. In particular the actual onset of SEL was at a higher LET in the Sapphire compared to the DNW Sapphire. The apparent disagreement between the data and the extracted parameter of LET threshold comes about from the fact that the shapes of the fitted curves (i.e. the  $W$  and  $S$  parameters) differ.

To explore this, the same data is plotted in Figure 8. This time however, weighted least-mean-squares fit amongst all data points in all three series has been found, with the condition that  $W$  and  $S$  are the same for every series. The resulting fitting parameters are shown in Table 4.

Device	$\sigma_0$ (latchups/ion/cm <sup>2</sup> )	$L_0$ (MeV.cm <sup>2</sup> /mg)	$W$ (MeV.cm <sup>2</sup> /mg)	$S$
Sapphire	$2.06 \times 10^{-3}$	9.08	34.4	4.21
DNW Sapphire	$2.66 \times 10^{-3}$	0.87	34.4	4.21
Ruby 18 $\mu$ m	$1.90 \times 10^{-3}$	13.6	34.4	4.21

Table 4. Fitting parameters which provide the curves in Figure 8. Here,  $W$  and  $S$  are kept constant for all three devices and are chosen to give the best fit overall.

From this analysis the order of the extracted saturation cross sections are reversed for the Sapphire and the DNW Sapphire. The effect of the addition of the deep n well can be seen as simply reducing the hardness of the devices to latchup, since the threshold LET is reduced. Alternatively, the deep n well can be seen as changing the characteristic shape of the LET vs. cross section curve such that the metric of threshold LET is no longer a useful tool for comparing the Sapphire and the DNW Sapphire.

It is possible that the deep n well has made the Sapphire more susceptible to latchup. The deep n well connects multiple n wells which reduces the resistance from  $V_{DD}$  to the pnp BJT base and reduces the pnp BJT gain. However, at the same time the deep n well has the opposite effect on the npn BJT. The base to

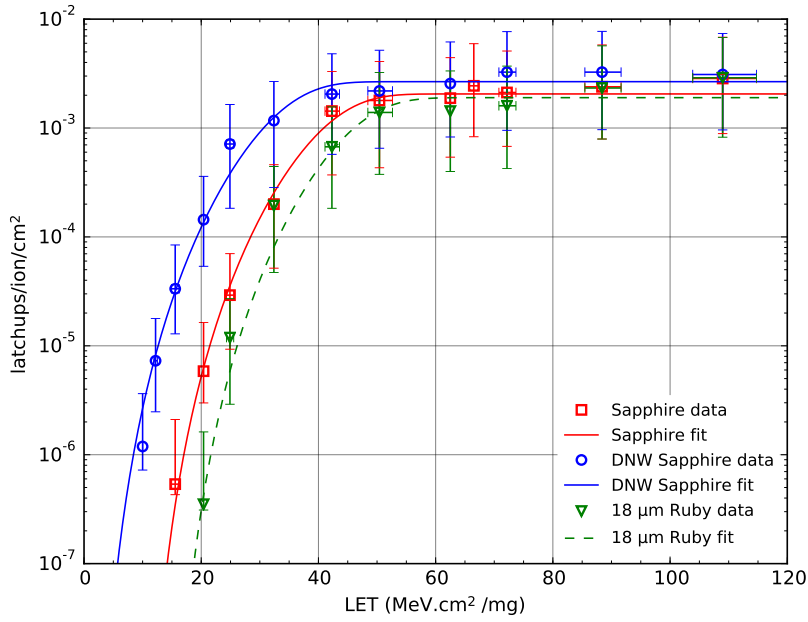


Figure 8. Here the Weibull fits to the data are calculated with  $W$  and  $S$  fixed across the three devices. Now all three curves have similar shapes, although the fits are not as good. The threshold LET is now higher for the Sapphire than for the DNW Sapphire which seems to represent the real data better. Once again the 18  $\mu\text{m}$  Ruby performs better than either the Sapphire or the DNW Sapphire.

$V_{SS}$  resistance, and the gain, of the npn BJT both increase. In the deep n well device studied in this work the latter effect may dominate, making SEL more probable. In the deep p well device the effects of reduced gain and resistance dominate, making SEL less probable.

In both analyses, the 18  $\mu\text{m}$  Ruby has an increased threshold LET and we therefore suggest that the use of a deep p well in order to reduce latchup susceptibility in this process is worthy of further study.

## 5. CONCLUSIONS

CMOS image sensors operating in the space radiation environment can be susceptible to single event latchup. Latchup occurs due to the doping structure and connections in CMOS devices. We have demonstrated how the susceptibility to latchup of real image sensors can be altered by using process modifications, namely the addition of deep n or wells and the adjustment of the epitaxial layer thickness. Often, such modifications can be performed with minimal redesign and without adding to the chip area. We produced the SEL cross sections of an e2v Sapphire using heavy ions up to a high LET. We also produced results for a Sapphire with a deep n well, and for a Ruby (which has identical circuitry) with a deep p well and a thicker epitaxial layer (18  $\mu\text{m}$ ).

From our analysis we are confident that Ruby device shows reduced susceptibility to SEL, as measured by the threshold LET. We are unable to say yet whether this improvement in performance is due to the epitaxial layer thickness, the epitaxial layer resistivity, the deep p well, or a combination of all three.

Our analysis of the Sapphire sensors has shown that the usual method of using a Weibull cumulative distribution fit to extract the threshold LET can lead to problems. A decision must be made as to whether or not the shape of the cross section vs. LET curve should be kept consistent across devices. This is an area of continuing investigation and we are performing TCAD simulations to show whether deep n wells can in fact change the shape of the curve, as well as the threshold LET. At this stage we are unable to make a conclusion as to whether the deep n well improved SEL hardness or not.

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